TECHNICAL NOTE

TN251

Rabbit 4000 16-bit Memory Wait State Bug

A bug has recently been identified in the Rabbit 4000 that can result in a missing wait state in certain circumstances. This missing wait state can lead to a missed or incorrect instruction byte depending on the characteristics of the memory being accessed.

It is highly unlikely that this bug will affect most customers because of the rare combination of conditions required for this bug to appear. There are several methods available to work around the issue that will not unduly affect code.

Description

A wait state may be missed when certain instructions transfer execution from a device operating in the advanced 16-bit mode to a device operating in a different memory interface mode. The exact circumstances that cause the missed wait state are complicated to predict because they involve the advanced 16-bit operating mode. In this mode a semi-autonomous prefetch mechanism fetches words from a 16-bit memory to feed to the instruction decoder. The fetched instruction bytes are presented to the instruction decoder on an as-needed basis, which is only loosely coupled to the operation of the external memory bus.

The bug can *only* occur if the following conditions are met.

1. One of these three instructions is used — JP (HL), JP (IX), or JP (IY).
2. The jump is from a memory using the advanced 16-bit mode into a memory that is not using the advanced 16-bit mode.
3. The destination memory requires wait states.

Whether the bug occurs is a function of when the instruction decoder accepts the JP instruction relative to the fetch of the next instruction on the bus. This in turn depends on both the instructions immediately prior to the JP instruction and the number of wait states used by the prefetch mechanism.

Workarounds

The simplest workaround is to not use the instructions listed above. The same operation can be handled by the following code sequence.

```
PUSH HL   ; or IX or IY
RET
```

This code sequence will obviously take more clocks to execute.

Another way to avoid the bug is to increase the number of wait states, if possible, on the device operating in the basic mode. Using this option will produce a loss of performance.

Finally, this bug can be avoided by not using the basic 16-bit mode unless absolutely necessary. It is highly likely that any SRAM device that you are executing code in will support the advanced 16-bit mode with byte-writes enabled, which will also improve the overall performance as a result of the 16-bit data fetches.