SYS TEC ELECTRONIC

ECUcore-5208

Hardware Manual

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L-1232e_1		initial version	M. Berthel
L-1232e_2		PCB version added	M. Berthel
	2	manual overview added	
	3	partnumbers added	

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1 Introduction

This manual describes the function and technical data for the ECUcore-5208. This manual does not cover the microcontroller Freescale Coldfire MCF5208 or any other supplemental components assembled on the ECUcore. Please refer to the corresponding manuals and documentation for any other products you may use.

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

This manual at time of printing is valid for the following hardware (PCB) versions:

- ECUcore-5208: 4218.2
- Development board: 4220.2

Declaration of Electro Magnetic Conformity for ECUcore-5208 (EMC law)

The ECUcore-5208 has been designed to be used as vendor part for the integration into devices (further industrial processing) or as Development Board for laboratory development (hard- and software development).

After the integration into a device or when changes/extensions are made to this product, the conformity to EMC-law again must be assessed and certified. Only thereafter products may be launched onto the market.

The CE-conformity is only valid for the application area described in this document and only under compliance with the following commissioning instructions! The ECUcore-5208 is ESD-sensitive and may only be unpacked, used and operated by trained personal at ESD-conform work stations.

2 Overview / Where to find what?

Information about…	In which manual?
Hardware description about the ECUcore-5208 / PLCcore-5208, reference designs et cetera	In this manual
Development Board for the ECUcore-5208 / PLCcore-5208, reference designs et cetera	Hardware Manual Development Board 5208 (Manual no.: L-1074)
Development of user-specific C/C++ applications for the ECUcore-5208 / PLCcore-5208, VMware-Image of the Linux development system	System Manual ECUcore-5208 (Manual no.: L-1202)
Basic information about the PLCcore-5208 (configuration, administration, process image, connection assignment, firmware update, reference designs et cetera)	System Manual PLCcore-5208 (Manual no.: L-1076)
Driver Development Kit (DDK) for the ECUcore-5208	Software Manual Driver Development Kit (DDK) for ECUcore-5208 (Manual no.: L-1231)

Table 1: Overview of relevant manuals for the ECUcore-5208

3 Ordering Information and Support

Part Number	Version
4001006	ECUcore-5208, standard version, uClinux
KIT-155	Development Kit ECUcore-5208, uClinux
3390014	PLCcore-5208/Z4 PLC, IEC 61131-3
3390015	PLCcore-5208/Z5 PLC, IEC 61131-3
KIT-158	Development Kit PLCcore-5208 PLC, IEC 61131-3
4002006	Developmentboard ECUcore-5208

The ECUcore-5208 standard version features:

- Freescale MCF5208 MCU with 166 MHz
- 4MiB NOR FLASH
- 64MiB NAND Flash
- 32MiB SDRAM
- 16kiB EEPROM
- Ethernet PHY
- SPI CAN controller
- Real-Time-Clock
- Reset-/Watchdog-IC
- Temperature-Sensor
- single power supply 3,3V (all other voltages are derived onboard)

We offer a complementary Development Board for the ECUcore-5208. This board will provide you a convenient hardware base for own application development. The Development Board offers the following functionality:

- power supply connector 9-24VDC and a external power supply
- Push-button and LEDs,
- Connectors for all module interfaces
- Ethernet-Interface
- Potentiometer with ADC
- DAC with LED
- Keypad connector
- LCD display connector
- BDM interface connector

- All board pins are accessible for on a pin-header field

Development Kit ECUcore-5208

The ECUcore modules are designed to be plugged onto applicable Development Boards. Both the module and Development Board are included in the Development Kit. The Development Board contains the I/O connectors required for immediate start-up of the module, as well as other interface circuitry not provided on the SBC module itself. The SBC, when mounted on the Development Board, provides an excellent platform with which to evaluate controllers, develop software, as well as specify and determine the feasibility of new embedded designs.The ECUcore-5208 Development Kit comes with the following contents:

- ECUcore-5208, bootloader and OS pre-installed
- Development Board ECUcore-5208
- Integrated Development Environment (Eclipse-based, GNU toolchain) pre-installed on a VMware Virtual Machine (VMware player to run the virtual machine is available free-of-charge for Windows platforms)
- • Board Support Package with uClinux OS and drivers
- • Documentation (PDF)
- • 90 days support via e-mail or phone
- • Accessories

Software packages

A Board Support Package on DVD is shipped with all Development Kits (SO-1096 - uCLinux Development System for ECUcore-5208). This DVD offers complete electronic documentation and demo programs. It also contains an enhanced Eclipse-based Integrated Development Environment, including a uClinux Operating System, Optimizing ISO C/C++ compiler and macro-assembler, a powerful linker with complete control of section placement and a Source- and assembly-level debugger. The Development Kit also includes a CANopen Library.

- Integrated Development Environment with complete GNU toolchain for ColdFire architecture (Eclipse-based)
- Colilo bootloader (pre-installed on target at time of delivery)

- uClinux operating system (pre-installed on target and source code on the VMware host system)
- CANopen Library including demo project
- CAN driver including demo project

4 Properties of the ECUcore-5208

4.1 Overview

The ECUcore-5208 is a member SYS TEC's ECUcore family. The ECUcore-5208 integrates all elements of a microcontroller system on a board. The module was designed for low-end to medium sized applications, that require a combination of various communication interfaces with and high computing power. Typical applications are point of sale, communication gateways or embedded machine controller.

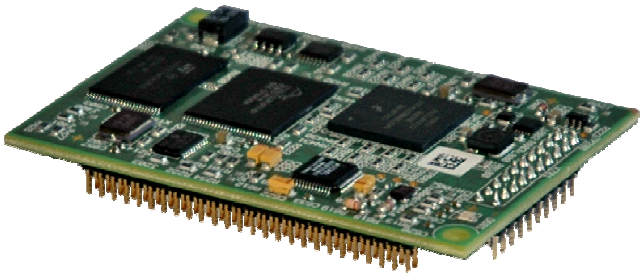

Figure 1: ECUcore-5208

The dimensions of the board are 72mm x 51mm and its two pin-header board connectors allow for easy integration in embedded applications.

The ECUcore-5208 includes a Freescale MCF5208 microcontroller. It is a highly-integrated 32-bit microprocessors based on the V2-core of ColdFire microarchitecture. It contains a 16kiB internal SRAM and 8kiB configurable cache.

The interconnection to a baseboard is allowed through a pair of 2mm pitch pin header connectors with summary 104 Pin.

The ECUcore-5208 offers the following features:

- Internal Features of the Freescale Coldfire MCF5208:
    - internal 166.67MHz CPU-clock
    - 32-bit bus interface (shared, SDRAM controller and Flexbus), demultiplexed
    - 10/100Mbps Fast Ethernet Controller
    - I2C bus
    - Queued SPI bus
    - 4 32-bit DMA timer
    - 2 Watchdog timer (CPU and hardware)
    - Periodic Interrupt Timer (PIT)
    - Interrupt Controller
    - external interrupts
    - 16-channel DMA
    - GPIO module
    - JTAG/BDM module
    - 196-pin BGA package
- Memory Configuration:
    - 4MiB NOR Flash-Memory
    - 64MiB NAND Flash-Memory
    - 32MiB SDRAM
    - 16kiB EEPROM

- Communication features:
    - 3 UARTs
    - 1 CAN
    - SPI
    - I²C
    - 1 Ethernet interface (PHY onboard)

- Other Board-Level Features:
    - Reset- and Watchdog-IC
    - Power failure recognition
    - real-time-clock
    - temperature sensor
    - JTAG/BDM module
    - 3.3V operating voltage
    - Industrial temperature range (-40°C to +85°C)
    - RoHS compliant

4.2 Block Diagram

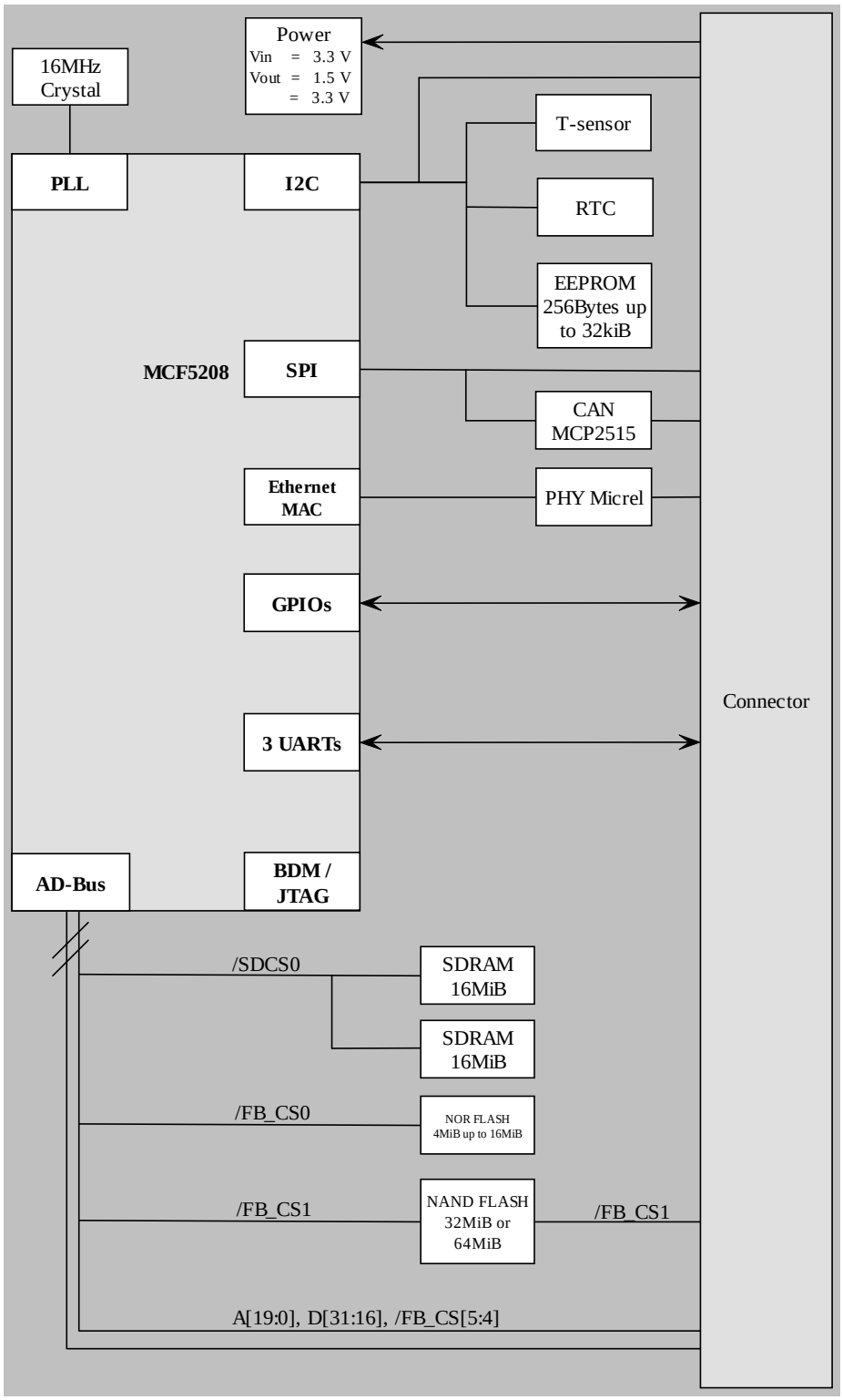

Figure 2: Block Diagram ECUcore-5208

5 Component Descriptions

The functions of the on-board components are explained in the following sections.

5.1 Pin-header Connection

The ECUcore-5208 has two board connectors. Each of the two SMT pin header strips consists of 52 contacts divided into double rows. In total the module has 104 pins.
A BDM/JTAG interface is brought out by drill holes (X701) with 20 contacts , a pitch of 2.54mm with a hole diameter of 1.5mm.

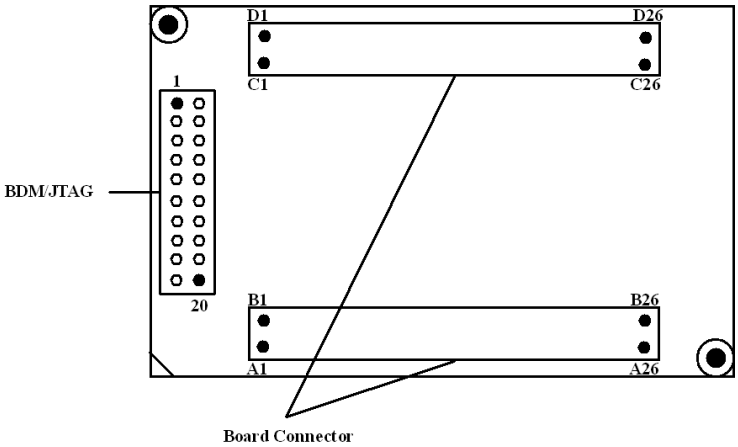

Figure 3: Pinout of the ECUcore-5208 (top view)

The pitch of the board connectors is 2.00mm. The pin header connectors equipped on the ECUcore-5208 are the 7351 series provided by W+P Products.

The series mates with W+P Products female header series 7450-52-20-xx-xx (x is user specific). Please refer to the connector datasheet for their electrical specifications.

The columns A and B representing connector 1. In addition the columns C and D representing connector 2. The position of the two connectors is fixed, so these components are summarized to X700.

Signal	Pin	Pin	Signal		Signal	Pin	Pin	Signal
GND	A01	B01	/MR		2V5_EPHY	C01	D01	ETH_TX-
/RSTO	A02	B02	/RSTI		GND	C02	D02	ETH_TX+
PFI	A03	B03	PI2C_DATA		ETH_RX+	C03	D03	ETH_LINK/ACT
WDI	A04	B04	GND		ETH_RX-	C04	D04	GND
TP_0	A05	B05	PI2C_CLK		ETH_SPEED	C05	D05	GPIO_PUART2
A0	A06	B06	A10		D16	C06	D06	D24
GND	A07	B07	A11		GND	C07	D07	D25
A1	A08	B08	A12		D17	C08	D08	D26
A2	A09	B09	A13		D18	C09	D09	D27
A3	A10	B10	GND		D19	C10	D10	GND
A4	A11	B11	A14		D20	C11	D11	D28
A5	A12	B12	A15		D21	C12	D12	D29
GND	A13	B13	A16		GND	C13	D13	D30
A6	A14	B14	A17		D22	C14	D14	D31
A7	A15	B15	A18		D23	C15	D15	PSPI_/CS2
A8	A16	B16	GND		PSPI_/CS0	C16	D16	GND
A9	A17	B17	A19		PSPI_/CS1	C17	D17	PSPI_/CSCAN
/CS1	A18	B18	/CS4		PSPI_CLK	C18	D18	PSPI_MRST
GND	A19	B19	/CS5		GND	C19	D19	GPIO_PIRQ1
R/W	A20	B20	/OE		PSPI_MTSR	C20	D20	GPIO_PIRQ7
/BWE0	A21	B21	GPIO_BWE1		GPIO_PTIMER 2	C21	D21	GPIO_PCS2
GPIO_PBUSCTL0	A22	B22	GND		GPIO_PTIMER 3	C22	D22	GND
GPIO_PBUSCTL2	A23	B23	/BOOTSELECT		PUART_RXD0	C23	D23	GPIO_PCS3
VBAT	A24	B24	PCAN_RX0		PUART_RXD1	C24	D24	PUART_TXD0
GND	A25	B25	PCAN_TX0		GND	C25	D25	PUART_TXD1
3V3	A26	B26	3V3		PUART_RXD2	C26	D26	PUART_TXD2

Table 2: Pinout of the ECUcore-5208

Pin	Signal	Function (alternate function)	Dir	On-board usage (only MCF5208-signals)	Transmitter /Receiver
A01	GND	Ground			
A02	/RSTO	Reset Output	O	Pull-Up	MCF5208
A03	PFI	Power Failure Input	I	Pull-Up	Reset-IC
A04	WDI	Watchdog Signal Input	I		Reset-IC
A05	TP_0	Testpoint 1.5V	O		Step-Down Regulator
A06	A0	Flexbus Address A0	O	Flash	MCF5208
A07	GND	Ground			
A08	A1	Flexbus Address A1	O	Flash	MCF5208
A09	A2	Flexbus Address A2	O	Flash	MCF5208
A10	A3	Flexbus Address A3	O	Flash	MCF5208
A11	A4	Flexbus Address A4	O	Flash	MCF5208
A12	A5	Flexbus Address A5	O	Flash	MCF5208
A13	GND	Ground			
A14	A6	Flexbus Address A6	O	Flash	MCF5208
A15	A7	Flexbus Address A7	O	Flash	MCF5208
A16	A8	Flexbus Address A8	O	Flash	MCF5208
A17	A9	Flexbus Address A9	O	Flash	MCF5208
A18	/CS1	Flexbus Chip Select 1	O	Pull-Up, optional NAND-Flash	MCF5208
A19	GND	Ground			
A20	R/W	Flexbus Read_/ Write	O	Flash	MCF5208
A21	/BWE0	Flexbus Byte Write Enable	O	SDRAM	MCF5208
A22	GPIO_PBUSCTL0	GPIO	I/O		MCF5208
A23	GPIO_PBUSCTL2	GPIO	I/O		MCF5208
A24	VBAT	RTC buffer supply	I	RTC	RTC
A25	GND	Ground			
A26	+3V3	3.3V supply voltage	I		
B01	/MR	Manual Reset	I	Pull-Up	Reset-IC
B02	/RSTI	Reset In	I	MCF5208, PHY, Flash, Pull-Up	Reset-IC
B03	PI2C_DATA	I2C data	I/O	EEPROM, RTC, Temp.sensor, Pull-Up	MCF5208
B04	GND	Ground			
B05	PI2C_CLK	I2C clock	I/O	EEPROM, RTC, Temp.sensor, Pull-Up	MCF5208
B06	A10	Flexbus Address A10	O	Flash	MCF5208
B07	A11	Flexbus Address A11	O	Flash	MCF5208
B08	A12	Flexbus Address A12	O	Flash	MCF5208
B09	A13	Flexbus Address A13	O	Flash	MCF5208
B10	GND	Ground			
B11	A14	Flexbus Address A14	O	Flash	MCF5208
B12	A15	Flexbus Address A15	O	Flash	MCF5208
B13	A16	Flexbus Address A16	O	Flash	MCF5208
B14	A17	Flexbus Address A17	O	Flash	MCF5208
B15	A18	Flexbus Address A18	O	Flash	MCF5208
B16	GND	Ground			
B17	A19	Flexbus Address A19	O	Flash	MCF5208
B18	/CS4	Flexbus Chip Select 4	O	Pull-Up	MCF5208

Pin	Signal	Function (alternate function)	Dir	On-board usage (only MCF5208-signals)	Transmitter /Receiver
B19	/CS5	Flexbus Chip Select 5	O	Pull-Up	MCF5208
B20	/OE	Flexbus Output Enable	O	Flash	MCF5208
B21	BWE1	Flexbus Byte Write Enable	O	SDRAM	Ethernet Phy
B22	GND	Ground			
B23	/BOOTSELECT	Boot Select Operating System and GPIO	I/O	Pull-Up	MCF5208
B24	PCAN_RX0	CAN-channel Rx	I		MCF5208
B25	PCAN_TX0	CAN-channel Tx	O		MCF5208
B26	+3V3	3.3V supply voltage	I	Peripherals	Peripherals
C01	+2V5_EPHY	supply voltage Ethernet	O		Ethernet Phy
C02	GND	Ground			
C03	ETH_RX+	Ethernet Receive Input +	I		Ethernet Phy
C04	ETH_RX-	Ethernet Receive Input -	I		Ethernet Phy
C05	ETH_SPEED	Ethernet Speed Output, 10BT high, 100BT low	O		Ethernet Phy
C06	D16	Flexbus Data D16	I/O	Flash	MCF5208
C07	GND	Ground			
C08	D17	Flexbus Data D17	I/O	Flash	MCF5208
C09	D18	Flexbus Data D18	I/O	Flash	MCF5208
C10	D19	Flexbus Data D19	I/O	Flash	MCF5208
C11	D20	Flexbus Data D20	I/O	Flash	MCF5208
C12	D21	Flexbus Data D21	I/O	Flash	MCF5208
C13	GND	Ground			
C14	D22	Flexbus Data D22	I/O	Flash	MCF5208
C15	D23	Flexbus Data D23	I/O	Flash	MCF5208
C16	PSPI_/CS0	SPI Chip Select 0, (GPIO)	I/O		MCF5208
C17	PSPI_/CS1	SPI Chip Select 1, (GPIO)	I/O		MCF5208
C18	PSPI_CLK	SPI Clock	O	CAN, Pull-Down	MCF5208
C19	GND	Ground			
C20	PSPI_MTSR	SPI Input (Master Transmit Slave Receive)	O	CAN, Pull-Up	MCF5208
C21	GPIO_PTIMER2	GPIO	I/O	Write Protect EEPROM, optional NAND-Flash, Pull Down	MCF5208
C22	GPIO_PTIMER3	GPIO	I/O		MCF5208
C23	PUART_RXD0	UART 0 Receive Input (GPIO)	I		MCF5208
C24	PUART_RXD1	UART 1 Receive Input (GPIO)	I		MCF5208
C25	GND	Ground			
C26	PUART_RXD2	UART 2 Receive Input (GPIO)	I		MCF5208
D01	ETH_TX-	Ethernet Transmit Output	O		
D02	ETH_TX+	Ethernet Transmit Output +	O		Ethernet Phy
D03	ETH_LINK/ACT	Ethernet Link-Activity, No Link	O		Ethernet Phy

Pin	Signal	Function (alternate function)	Dir	On-board usage (only MCF5208-signals)	Transmitter /Receiver
		high, Link low, Act toggle			
D04	GND	Ground			
D05	GPIO_PUART2	GPIO	O		MCF5208
D06	D24	Flexbus Data D24	I/O	Flash	MCF5208
D07	D25	Flexbus Data D25	I/O	Flash	MCF5208
D08	D26	Flexbus Data D26	I/O	Flash	MCF5208
D09	D27	Flexbus Data D27	I/O	Flash	MCF5208
D10	GND	Ground			
D11	D28	Flexbus Data D28	I/O	Flash	MCF5208
D12	D29	Flexbus Data D29	I/O	Flash	MCF5208
D13	D30	Flexbus Data D30	I/O	Flash	MCF5208
D14	D31	Flexbus Data D31	I/O	Flash	MCF5208
D15	PSPI_/CS2	SPI Chip Select CAN	O	CAN	MCF5208
D16	GND	Ground			
D17	PSPI_/CSCAN	SPI Chip Select CAN	I/O	CAN	MCF5208
D18	PSPI_MRST*	SPI Output (Master Receive Slave Transmit)	I	CAN, Pull-Up	MCF5208
D19	GPIO_PIRQ1*	external Interrupt 1 (GPIO)	I	PFI, Pull-Up	MCF5208
D20	GPIO_PIRQ7*	external Interrupt 7 (GPIO)	I	CAN, Pull-Up	MCF5208
D21	GPIO_PCS2	GPIO	I/O		MCF5208
D22	GND	Ground			
D23	GPIO_PCS3	GPIO	I/O		MCF5208
D24	PUART_TXD0*	UART 0 Transmit Output (GPIO)	O		MCF5208
D25	PUART_TXD1*	UART 1 Transmit Output (GPIO)	O		MCF5208
D26	PUART_TXD2*	UART 2 Transmit Output (GPIO)	O		MCF5208

Table 3: ECUcore-5208 pin description

5.2 Jumper Configuration

On default the jumpers are configuered for a proper function of module. Change positions only if you really need it in a special application!
The following figure shows the positions of jumpers. All placed on top-side of module.

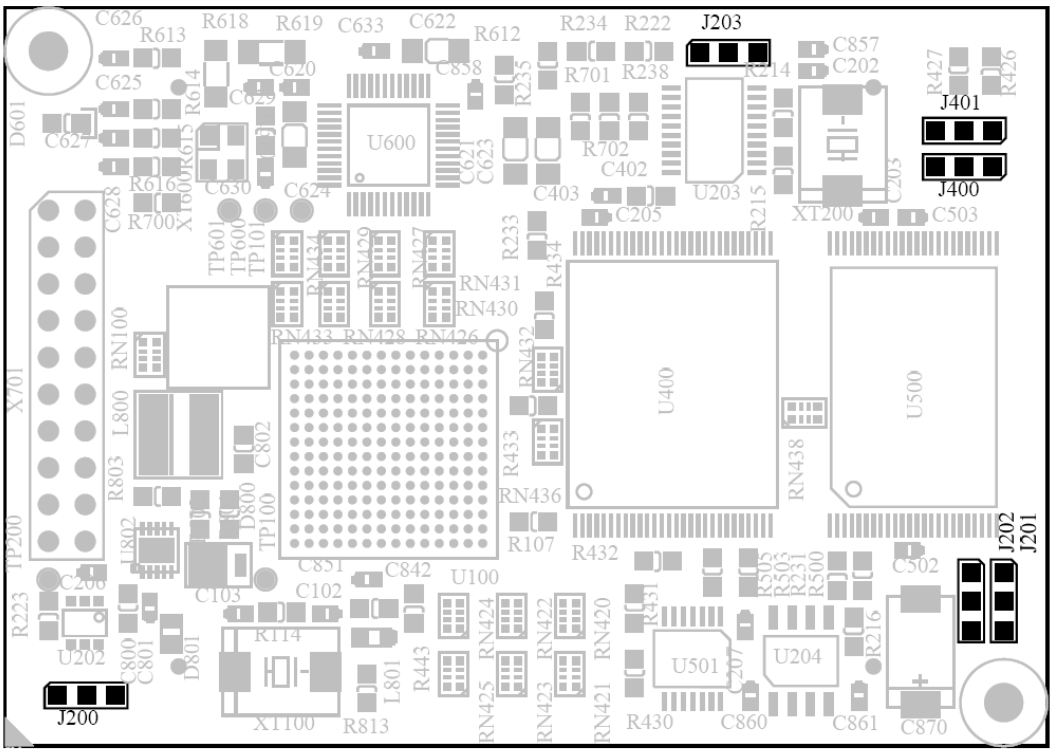

Figure 4: Jumper positions

The following table lists each solder jumper and its function on the ECUcore-5208.

Jumper	Jumper Pad Setting	Function
J200	open	I2C address of temp. sensor is 1001001b
	1-2	I2C address of temp. sensor is 1001010b
	2-3 (default)	I2C address of temp. sensor is 1001000b
J201	1-2 (default)	A2 of EEPROM I2C address is 1b
	2-3	A2 of EEPROM I2C address is 0b
J202	1-2	EEPROM is write protected
	2-3 (default)	normal read/write operation of EEPROM
J203	1-2 (default)	/RXB0BF is connected to /BOOTSELECT
	2-3	/RXB0BF is connected to /GPIO:PBUSCTL2
J400	1-2(default)	D5: High output pad drive strength
	2-3	D5: Low output pad drive strength
J401	1-2 (default)	D9: A[23:22] = /CS[5:4]
	2-3	D9: A[23:22] = A[23:22]

Table 4: Overview of the Solder Jumpers and Default Settings

If you need additional information or advice on the above jumper settings please contact our support.

5.3 Power Supply

Board Supply

The ECUcore-5208 must be supplied with an input voltage of +3.3V DC. The MCU core itself runs at a voltage of 1.5V DC, which is generated by the on-board step-down regulator.

- Rated voltage VCC: +3.3V DC ±9%
- Max. voltage VCC_max: +3.6V DC
- Min. voltage VCC_min: +3.0V DC

Battery Backup (RTC)

The Real-Time Clock can be battery-backed using VBAT pin (A24) to keep the system time while the board is powered off. The RTC has an supply voltage range of 1.8V DC to 5.5V DC and features a protection diode and 10% buffer zone with the following specifications:

- Rated voltage range VBAT: +2.4V ≤ +3.3V ≤ +5.5V
- Max. voltage VBAT_max: +5.5 V DC
- Min. voltage VBAT_min: +2.4 V DC

Onboard voltages

The onboard switching regulators generate all the other needed voltages. These are:

- 1,5V for Coldfire Core
- 2,5V for Ethernet PHY and LAN

5.4 Reset Characteristics

The Sipex Supervisory Circuit SP706T is used to define the reset characteristics and generates the system reset signal /RSTI.
The reset in signal (/RSTI) is low-active and connected to a pull-up resistor.

It asserts a reset on the following conditions:

- Power supply voltage VCC drops below 3.08V
- Manual reset (/MR) voltage drops below 0.6V
- WDI pin: no signal occured within a timespan of 1,6s

An internal timer releases /RESET after 200ms. When a brownout condition occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. During reset the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven HIGH or LOW, the timer will start counting. It can detect pulses starting with a minimum pulse width of 50ns.

The Power Fail Input signal (PFI) should be more than 1.25V to produce a high-level on /PFO. When PFI voltage monitor input is less than 1.25V, /PFO goes low. The signal /PFO is connected to external interrupt GPIO_PIRQ1. PFI is pulled up to 3,3V with 1MOhm.

5.5 Chip Configuration after Reset

The Chip Configuration is managed by the /RCON pin. If the external /RCON pin is asserted during reset cycle, then the state of the data pins D[9,5] during reset are used to define the MCU's reset configuration.
By layout setting /RCON is fixed to low-level. Therewith the values from the table below are used.

The following table shows the default configuration during reset:

Override Pins in Reset	Function	Pin(s) affected
D1	**Processor Clock**	
1	Clock is 166,67MHz	
D2	**Oscillator Mode**	
0	Crystal Oscillator Mode	
D3, D4	**Boot device**	
00	16bit boot device	
D5 (J400)	**Output pad drive strength**	**All output pins**
0	Low drive strength	
1	High drive strength	
D6	**PLL Mode**	
0	Normal PLL Mode	
D7	**Input Clock**	
0	16MHz Input Clock	
D9 (J400)	**Chip Select Configuration**	**A[23:22] / / FB_CS[5:4]**
0	A[23:22] = A[23:22]	
1	A[23:22] = /FB_CS[5:4]	

Table 5: Reset configuration

The user can change the signals D9 and D5 via jumpers J401 and J400 (see also Table 4). The light-grey background indicates the default configuration at time of shipment.

Description of config options

Output Pad Strength Configuration:
The pad drive strength is selected by data pin D5. By default it is set to high drive strength.

Chip Select Configuration:
During reset the chip select configuration is selected by data pin D9. By default A[23:22] is set to /CS[5:4].

For further information of config options see Reference Manual of MCF5208.

5.6 Memory

The memory range of the ECUcore-5208 is divided into an internal and external memory. The MCF5208 has a 16kiB internal SRAM, which can be used as the system stack for example. The external memory interface is shared between the on-chip SDRAM controller and the Flexbus. The Flexbus connects the NOR Flash and NAND Flash to the CPU.
Additionally an on-board EEPROM device is accessible via I2C bus.
Please refer to Freescale MCF5208 Reference Manual for more information on overall device memory map.

Memory mapping:

Module	Address Range	Size
Flexbus	0x00000000 - 0x3FFFFFFF and 0xC0000000 - 0xDFFFFFFF	1024MBit
		512MBit
SDRAM Controller	0x40000000 - 0x7FFFFFFF	1024MBit
Internal SRAM	0x80000000 - 0x8FFFFFFF	256MBit
On-chip Peripheral Controller 0	0xF0000000 - 0xFFFFFFFF	256MBit

Table 6: Memory mapping

Chip select configuration:

CS	Device	Size	Bus width
/CS0	NOR FLASH	4MiB	16-bit
/CS1	NAND FLASH	32MiB or 64MiB	8-bit
/SDCS0	SDRAM	16MiB or 32MiB	16-bit or 32-bit

Table 7: Chip select configuration

The memory data port size of SDRAM is controlled by the SDRAM Control Register (SDCR). The memory data port size of the Flexbus is controlled by the Chip Select Control Register (CSCRn). The “n” represents the corresponding chip select.

5.6.1 SDRAM interface

The external data bus is shared between the Flexbus module and the SDRAM controller. When the SDRAM controller is in SDR mode (DRAMSEL = 1), the data bus is switched dynamically between the SDRAM controller and the Flexbus module.
The state of the DRAMSEL pins is sampled at reset to select between the two modes. When DRAMSEL is high, the 32-bit bus mode is selected. D[31:0] switches dynamically between SDRAM and Flexbus accesses as needed. By default DRAMSEL is pulled high.
By default the ECUcore-5208 equips 32MiB SDRAM with 32-bit bus architecture. That means, there are two SDRAM devices (U300, U301) of 16 MiB size and 16-bit wide access, what are connected to data lines D[31:0], address lines A[15:14, 12:0] and SDRAM Chip Select /SDCS0.
As an assembly option it is possible to equip the board with only one 16MiB device at data lines D[31:16] resulting in operating the SDRAM with a 16-bit wide bus access (lower performance).

5.6.2 Flexbus interface

A multi-function external bus interface called the Flexbus interface controller is provided on the device. It can be directly connected to asynchronous or synchronous devices, such as external boot ROMs, Flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. Chip select /CS0 is connected to the 16-bit wide boot ROM (FLASH U400).
After system reset, /CS0 is asserted for every external access. No other chip select can be used until the valid bit CSMR0[V] is set, at which point /CS0 functions as configured. After this, /CS[5:1] can be used as well. At reset, the port size of the global chip select is determined by the logic levels on the D[4:3] signals. The port size is fixed and cannot be changed by the user.

5.6.3 Flash memory

The ECUcore-5208 comes with a default 4MiB NOR-FLASH (16-bit architecture) device. Additional the ECUcore-5208 is equipped with a 64MiB NAND-FLASH device.

NOR Flash

The standard equippment of NOR-FLASH (U400) is about 4MiB with 16-bit wide access. It is connected to data lines D[31:16], address lines A[23:1] and Chip Select /CS0. The flash has an access time of 90ns. The footprint of U400 is for device number S29GL128P90TFIxx to populate a maximum density of 16MiB.

NAND Flash

The ECUcore-5208 is equipped with a 8-bit NAND-FLASH. NAND-FLASH devices can be connected to a microcontroller system bus for program and data storage. By default the ECUcore-5208 is equipped with a 64MiB device. The NAND-FLASH is connected to data lines D[31:24] using a 8-bit architecture. The equipped NAND flash type is: ST Microelectronics NAND512W3A2BN6

5.7 Ethernet Controller

The ECUcore-5208 supports 10/100 Ethernet through the on-board PHY chip KSZ8721BLI from Micrel. The MII to the PHY chip is connected to MCF5208 MII serial management unit, allowing the microcontroller control the PHY.

The following Ethernet signals are available on the board connector:

Signal	description
Eth0_Tx+	Tx+ from PHY
Eth0_Tx-	Tx- from PHY
Eth0_Rx+	Rx+ from PHY
Eth0_Rx-	Rx- from PHY
2V5_EPHY	2,5V PHY-Supply (output of PHY)
Link/Act	output for link/act LED (parallel a yellow LED is mounted on board with 270R)
Speed	output for Speed LED

Table 8: Ethernet Signals

The Ethernet Controller defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the Fast Ethernet Controller. On the ECUcore-5208 with µCLinux this is done by the operation system at start up.

MAC Address

Each Ethernet Controller has it's unique MAC address. SYS TEC electronic has aquired a pool of these MAC addresses and assignes a MAC address to every ECUcore-5208 delivered with the Development Kit.
You can find the MAC address printed on the barcode label attached on the Development Kit box or on the ECUcore-5208 module.
Serial modules of the ECUcore-5208 that are intended for deployment in customer applicats are shipped without MAC address. If you need a SYS TEC MAC address assigned for the serial modules please contact our support or sales prior ordering the modules.

5.8 I2C-Module

The ECUcore-5208 features a 2-wire serial bus I2C interface, used for communication with I2C devices. The I2C bus connects the on-board Real Time Clock (RTC), Temperature sensor and EEPROM to the CPU. The bus is also brought out on the board connector. The three on-board I2C devices with their respective addresses are listed in the table below.

I2C device / type	I2C address
Real-Time-Clock [Epson 8564JE (U201)]	0xA2
Temperature-Sensor [TI TMP101 (U202)]	0x48 (default)0x49 and 0x4A available upon request
EEPROM [Atmel AT24C128 (U204)]	0x50

Table 9: I2C addresses

All I2C devices have a fixed unique device number for each device built into them. The chip selection on the I2C bus is executed when the communication starts and the device number is sent from I2C bus as a slave address. The receiving device response to the communication only if it matches the slave address.

The pins of the I2C module defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the I2C module. On the ECUcore-5208 with µCLinux this is done by the operation system at start up.

5.8.1 Real Time Clock

The ECUcore-5208 is equipped with a Real Time Clock (RTC) providing a hardware time base. The device offers functions such as calendar clock, alarm and timer. It also outputs pre-defined frequencies (32.768kHz, 1024Hz, 32Hz, 1Hz) via the CLKOUT pin. The RTC connects to the CPU via I2C bus.

RTC Characteristics:

The RTC has the following characteristics:

- Built-in crystal running at 32.768 kHz
- programmable alarm, timer and interrupt functions
- low power consumption:
  - Bus active: ≤ 1mA
  - Bus inactive, CLKOUT inactive: ≤ 1µA
- Backup battery support (external via VBAT signal)

On the development board the Real Time Clock is supplied by 3.3V DC. If the system voltage fails, a backup battery connected to VBAT on X700/A24 can supply the RTC.

- I2C device addresses:
  - 0xA2 when write mode
  - 0xA3 when read mode

The RTC's clock output is always active. By default the regular frequency output is enabled which is connected to CPU pin PIRQ4. An interrupt function such as timer or alarm is optional via device pin /INT and CPU pin PIRQ4.

5.8.2 Temperature Sensor

The ECUcore-5208 supports assembly of an optional temperature sensor of type TMP101 (U202) to measure ambient temperature to, e.g, enable protection from overheating. The TMP101 connects to the CPU via I2C bus. The address can be changed via the on-board jumper J200

Device characteristics:

The TMP101 temperature sensor has the following characteristics:

- Temperature resolution of 0.0625°C
- Temperature range of -55°C to +125°C
- Alert pin as interrupt source if temperature exceeds defined limits (function shared with CAN)

By default the low-active alert pin is not connected to CPU GPIO_PIRQ7. If the CAN controller (U203) is present, the temperature sensor alert pin function is not available.

5.8.3 EEPROM

The ECUcore-5208 is equipped with a 16kBytes EEPROM AT24C16 device (U204). The EEPROM is connected to the CPU via I2C interface. The address can be changed via the on-board jumper J202

5.9 QSPI Interface

The ECUcore-5208 allows high-speed serial communication with SPI devices such as the on-board CAN controller. The QSPI bus signals are brought out via the board connector.

Chip select configuration

The following table shows the SPI signals available.

SPI signal	Decription
PSPI_/CS0	Chip Select 0, to board connector
PSPI_/CS1	Chip Select 1, to board connector
PSPI_/CS2	Chip Select 2, to board connector
PSPI_/CSCAN	Chip Select for CAN controller, brought to board connector too

Table 10: SPI chip select signals

The QSPI module defaults to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the QSPI module. On the ECUcore-5208 with µCLinux this is done by the operation system at start up.

5.10 CAN Controller

The ECUcore-5208 supports the optional assembly with the Microchip MCP2515 CAN controller. The MCP2515 interfaces with microcontrollers via the Serial Peripheral Interface. Microchip MCP2515 is a stand-alone Controller Area Network controller that implements CAN according to ISO 11898-1.
The following table shows the pinout connection between the CPU and the CAN controller.

Signal at the CAN-Controller	Signal at the MCF5208	Description
SO	SPI_MRST	Serial Output CAN controller
SI	SPI_MTSR	Serial Input CAN controller
SCK	SPI_CLK	Clock CAN controller
/CS	SPI_/CS1	Chip Select CAN controller
RXB0BF	U1CTS	Buffer 0 received
RXB1BF	TS/DACK0	Buffer 1 received

Table 11: CAN controller signals

By default the CAN controller provides an interrrupt line to the CPU via signal GPIO_PIRQ7. The board does not provide any CAN transceiver. A CAN transceiver is equipped on the Development Board.

5.11 UART Modules

The ECUcore-5208 supports up to 3 independent UARTs available on the board connector. They are used to interface serial communication via RS232 or RS422 level signals on development board. The following table shows the pinout. However, the ECUcore does not provide any on-board transceiver.

Signal MCF5208	Description
PUART_RXD0	Receiver serial data inputs UART0
PUART_TXD0	Transmitter serial data outputs UART0
PUART_RXD1	Receiver serial data inputs UART1
PUART_TXD1	Transmitter serial data outputs UART1
PUART_RXD2	Receiver serial data inputs UART2
PUART_TXD2	Transmitter serial data outputs UART2

Table 12: UART signals

The UART-Modules default to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the UART module. On the ECUcore-5208 with µCLinux this is done by the operation system at start up.

5.12 DMA Timers

Altogehter there are four 32-bit DMA Timers on the MCF5208. By default the ECUcore-5208 has one timer, GPIO_TIMER3. It is possible to expand the timers from one to four (extra TIMER0, TIMER1 and TIMER2). Please notice that the additional timers are not available as long as the UART2 and Write Protect of the EEPROM (U204) is used.
Each timer has 2 signals (input capture/output compare) multiplexed onto a single pin. At a time only one function, either TimerIn or TimerOut, can be enabled. The following table shows the pinout of this module.

Signal at the MCF5208	Default Function	Alternate Function
PUART_TXD2	Transmitter serial data outputs UART2	TIMER0
PUART_RXD2	Receiver serial data inputs UART2	TIMER1
GPIO_PTIMER2	Write Protect EEPROM	TIMER2
GPIO_PTIMER3	GPIO	TIMER3

Table 13: Timer signals

The PAR_TIMER register controls the functions of the DMA timer pins.

The DMA Timers default to GPIO after reset. The GPIO module must be configured to enable the peripheral function of the appropriate pins prior to configuring the DMA Timers.

5.13 BDM/JTAG Port

The ECUcore-5208 provides a BDM and a JTAG interface respectively. Both are brought out via the through-hole pad field (X701) on the short side of the ECUcore-5208 board. You can choose between these two interfaces by setting the JTAG_EN pin:

- JTAG mode (JTAG_EN = 1)
- Background Debug Mode (BDM) (JTAG_EN = 0)

By default the JTAG_EN is low to enable BDM function. If JTAG is enabled, the JTAG signals of the ECUcore-5208 are available on X701.
The ECUcore-5208 has a specific BDM/JTAG pinout on the short side of the board. The following table shows the pinout of the ECUcore-5208 debug port.

Pin	Signal	Pin	Signal
1	+3V3	11	PST2
2	+1V5	12	PST3
3	JTAG_EN	13	DDATA0
4	/BKPT_TMS	14	DDATA1
5	PSTCLK_TCLK	15	DDATA2
6	DSI_TDI	16	DDATA3
7	DSO_TDO	17	/TA
8	DSCLK_/TRST	18	/RSTI
9	PST0	19	GND
10	PST1	20	GND

Table 14: Pinout debug module

Pin 3 is occupied by signal JTAG_EN. By default the signal is low-level to enable the BDM function.

5.13.1 BDM

Background Debug Mode debugging makes it possible for a BDM debugger to have total control of the processor. In BDM, the processor complex (including DMA and timers) is halted and a variety of commands can be sent to the processor to access memory, registers, and peripherals.

Signal description

Signal	Description
Development Serial Clock (DSCLK)	Clocks the serial communication port to the debug module during packet transfers
Development Serial Input (DSI)	input that provides data input for the serial communication port to the debug module
Development Serial Output (DSO)	Provides serial output communication for debug module responses
Breakpoint (/BKPT)	Assertion of /BKPT puts the processor into a halted state after the current instruction completes, low-active
PSTCLK	PSTCLK indicates when the development system should sample PST and DDATA values
Debug Data (DDATA[3:0])	These output signals display the register breakpoint status as a default, or optionally, captured address and operand values
Processor Status (PST[3:0])	These output signals report the processor status

Table 15: BDM signals

The 26-pin BDM connector pinout is shown in the table below (recommended Berg connector pinout arranged 2×13). This connector is located on the development board.

The following table shows the BDM/JTAG layout with pin names.

Signal	Pin	Pin	Signal
not connected	1	2	/BKPT – TMS
GND	3	4	DSCLK – /TRST
GND	5	6	TCLK
/RSTI	7	8	DSI – TDI
3,3V	9	10	DSO – TDO
GND	11	12	PST3
PST2	13	14	PST1
PST0	15	16	DDATA3
DDATA2	17	18	DDATA1
DDATA0	19	20	GND
not connected	21	22	not connected
GND	23	24	PSTCLK
COREvoltage	25	26	/TA

Table 16: BDM/JTAG connector

5.13.2 JTAG

The core provides a debug interface called JTAG for boundary-scan testability, which helps with system diagnostic and manufacturing testing. This interface provides debug capability with five external control signals.

Signal description:

Signal	Description
TDO	Test Data Out
TDI	Test Data In
TMS	Test Mode Select
TCK	Test Clock
/TRST	Test Reset (low-active)

Table 17: JTAG signals

6 Technical Data

The physical dimensions of the ECUcore-5208 are shown in the figure below.

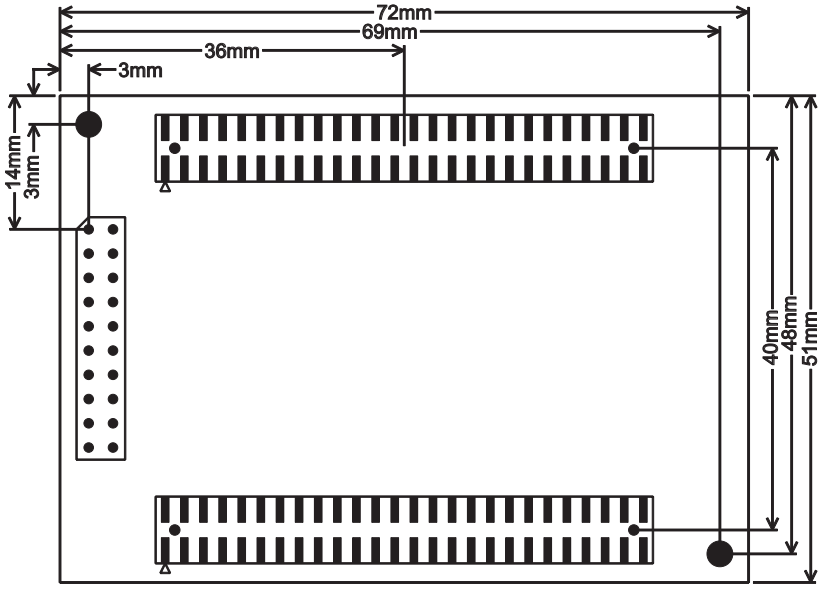

Figure 5: Dimensions

The height (from Development Board) including board connector and components is about 11.5mm. The thickness of the PCB is about 1.6mm. The maximum component height on top is about 3mm and 7mm on bottom.

- Dimensions: 72mm x 51mm
- Weight: approximately 20g
- Operating temperature: -40°C to +85°C
- Storage temperature: -40°C to +105°C
- Operating voltage: +3.3V DC ± 9%
- Power consumption: approximately 2.2W

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