QRT semiconductor

Reliability Test Report

QRT semiconductor, accredited laboratory of KOLAS(Korea Laboratory Accreditation Scheme), assists you in developing and assessing custom products. Reliability test procedures are recognized internationally by KOLAS certification, Mutual Recognition Arrangement .

COMPANY	:	***WIZnet Co. Ltd.***
PRODUCT	:	***W5300***
PACKAGE	:	***100 TQFP***
DOCUMENT No.	:	***CRRP-1103-00058***
ISSUED DATE	:	***May 13, 2011***

Prepared by ***N. H. Kim***

Reviewed by ***M. G. Kim***

Approved by ***M. Y. Park***

1 Qualification Plan and Results

The purpose of these tests is evaluation (or monitoring) of *W5300.*
Test conditions are specified in customers in-house test plan and all test procedures comply with JEDEC standards.
Obligation to perform exact procedure to reference documents is QRT semiconductor responsibility only, but establishing failure criteria and judgment of pass/fail is customer's responsibility.

TEST ITEM	TEST CONDITION	TEST TIME	SAMPLE SIZE	FAILED UNIT [1]	REF. DOCUMENT [2]
High temperature Operating Life	125 ℃, VCC3V3(V0) = 3.3 V VCC1V8(V4) = 1.8 V VIH = 3.3 V	504 h	77	0	JESD22-A108C

Additional Requirements: N/A

NOTE:
[1] This report may include test results that are not made by QRT but an examination agency designated by customers.
[2] Although the name of test item is same, reference documents can be JEDEC, MIL-std or AEC.

2 Test Vehicles

Manufacturer :	*WIZnet Co. Ltd*
Part Number :	*W5300*
Description :	-
Package Type :	*100 TQFP*
Sample Size:	*77 ea*
Ass'y Site :	-
Fab Site :	-

3 Test Flow/Procedure

All reliability Tests performed by QRT semiconductor was ensured with KOLAS accreditation. Entire test schematics are the same as below.

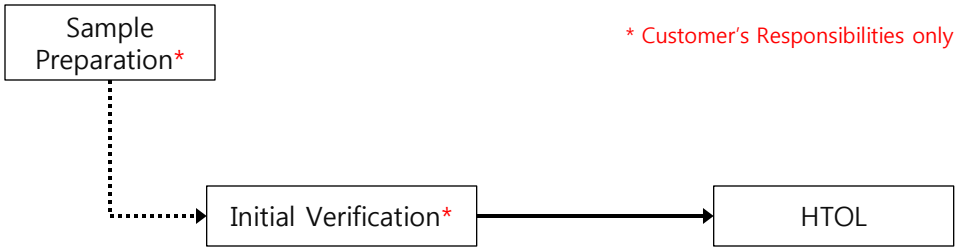


Figure 1. Reliability Test Flow

Final verification (Parametric and functional testing) is perform, after completion of each test.

4 Reliability Tests

4.1 High Temperature Operating Life test (HTOL)

The High Temperature Operating Life (HTOL) or steady-state life test is performed to determine the reliability of devices under operation at high temperature conditions over an extended period of time. It consists of subjecting the parts to a specified bias or electrical stressing, for a specified amount of time, and at a specified high temperature .

Conditions			
User Temp (T_U)	55 ℃	Test Temp (T_A)	125 ℃
User Voltage (V_U)	-	Test Voltage (V_A)	-
Activation Energy (E_{aa})	0.7	$\gamma V = (K/X)$	-
Sample size (N)	77	failures (f)	0
Test duration (t_A)	504	t_{life} (for ppm)	12 months

Life estimate is calculated on the assumption that 1) Gate short to source or drain *, 2) User temp is 55 ℃.
*Failure Mode: Gate short to source or drain
*Failure Mechanism: Intrinsic breakdown; for gate oxide thickness >4 nm
* E_{aa} = 0.7 (activation energy reference “JEP122D”)

---------Calculation----------

Acceleration Factor (AF) $= \exp\{(E_{aa}/k)(1/T_{use} - 1/T_{test})\}$
where
Eaa = apparent activation energy in eV/atom
k = Boltzmann’s constant (8.62×10^{-5} eV/K)
T_{use} = use temperature in kelvins
T_{test} = Test temperature in kelvins

$= \exp[(0.7/k) \times (1/328 – 1/398)] = 77.94$
∴ Test time = AF × Test Time = 77.94 × 504 = 4.48 years

if Exponential distribution (FIT Calculation)
The degrees of freedom = 2, and $\chi^2 = 1.83$ @ CL 60%
Failure rate (in FIT) = $10^9 \times \chi^2_{c,d} / (2 \times AF \times N \times t_A)$
$= 10^9 \times 1.83 /(2 \times 77.94 \times 77 \times 504) = 303$ FIT

∴ Failure Rate (in ppm, 12 months) = 2689 ppm during the first 12 months of usage.
∴ MTTF = 371.9 years

! Disclaimer !
This estimation is an example of JESD74A. Voltage Acceleration is excluded in this procedure.
Voltage acceleration and actual use temperature must be considered for a better output.
Calculation is for information only.

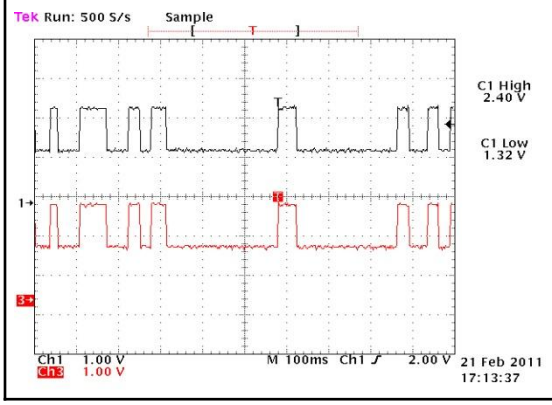
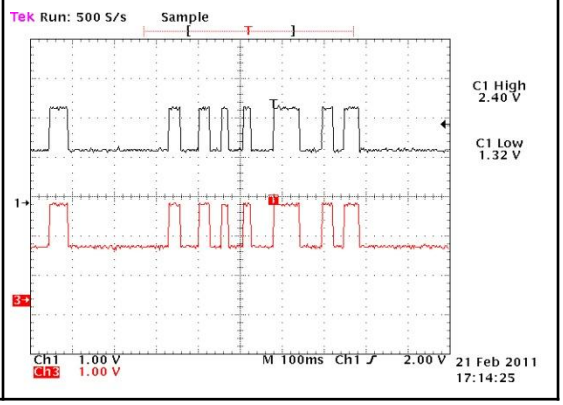
APPENDIX A: HTOL Conditions

a. HTOL Configuration

HTOL Board Density : 80ea / 2 Board	Load S/S : 77 ea / 2 Board
VCC3V3 (V0) : 3.3 V VCC1V8 (V4) : 1.8V	VIH : 3.3 V VIL : 0 V
Vector Type : ATPG_SEQ.ftl + ATPG_short.ftl + scan_chain.ftl	Cycle Time : 1000 ns
Timing Format Condition	
* Signal Rate : 1000 ns * Frequency : 1 MHz * ADDR9" { force { format RZ; start 150 , stop 500ns; } } * ADDR8" { force { format RO; start 150; stop 500; } }	

APPENDIX A: HTOL Conditions (cont'd)

b. Output signal

RXIN(#6) / RXIP(#5)	TXON(#9) / TXOP(#8)
	

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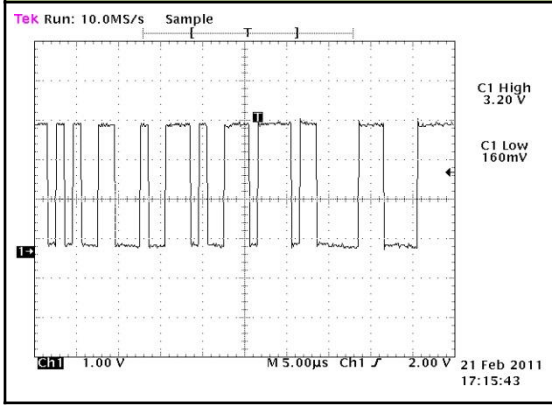	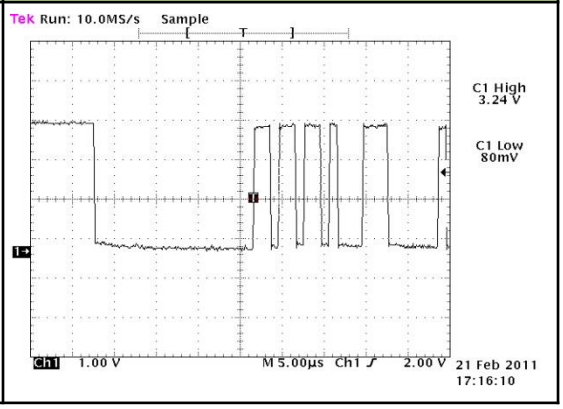

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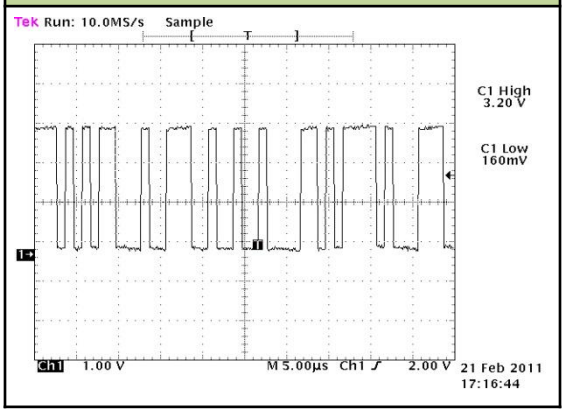

World Class Reliability Testing & Failure Analysis Company

Ichon Head Office…….……San 136-1 Ami-ri Bubal-eup Ichon-si Kyoungki-do, 467-701
Tel. 82-31-639-7684, 7617 Fax 82-31-639-7654

Cheongju Branch…….……1 Hyangjeong-dong Hungduk-gu Cheongju-si Chung buk, 361-725
Tel. 82-43-270-2748, 7128 Fax 82-43-270-2653

Gumi Branch……...……171 Imsoo-dong Gumi-si Kyung buk, 730-723
Tel. 82-54-470-1528, Fax 82-54-472-8031

Marketing (Ichon)
Tel. 82-31-639-7684 (7621)
doseok.ahn@qrtkr.com
dongsung.kim@qrtkr.com